L Number	Hits	Search Text	DB	Time stamp
1	46	(advanced adj micro adj devices) and dislocation	USPAT; US-PGPUB	2004/10/27 08:16
2	43	((advanced adj micro adj devices) and dislocation) and @ad<20020228	USPAT; US-PGPUB	2004/10/27 08:12
3	3	(advanced adj micro adj devices) and dislocation	EPO; JPO; DERWENT; IBM_TDB	2004/10/27 08:15
4	76	438/48,155,162,164,166,174,186.ccls. and dislocation	USPAT; US-PGPUB	2004/10/27 08:18
5	76	(438/48,155,162,164,166,174,186.ccls. and dislocation) not (((advanced adj micro adj devices) and dislocation) and @ad<20020228)	USPAT; US-PGPUB	2004/10/27 08:17
6	44	257/156,291,292,443,446,461.ccls. and dislocation	USPAT; US-PGPUB	2004/10/27 08:20
7	44	(257/156,291,292,443,446,461.ccls. and dislocation) not ((438/48,155,162,164,166,174,186.ccls. and dislocation) not (((advanced adj micro adj devices) and dislocation) and @ad<20020228))	USPAT; US-PGPUB	2004/10/27 08:20
8	44	((257/156,291,292,443,446,461.ccls. and dislocation) not ((438/48,155,162,164,166,174,186.ccls. and dislocation) not (((advanced adj micro adj devices) and dislocation) and @ad<20020228))) not (((advanced adj micro adj devices) and dislocation) and @ad<20020228)	USPAT; US-PGPUB	2004/10/27 08:20

US-PAT-NO: 6235599

DOCUMENT-IDENTIFIER: US 6235599 B1

TITLE: Fabrication of a shallow doped junction having low sheet resistance using multiple implantations

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Brief Summary Text - BSTX (14):
For implantation of the relatively heavy dopant species, a high implantation energy may be used. However, with a high implantation energy, the amorphization implant profile 200 may be buried beneath the top surface 130 of the semiconductor substrate 102, as illustrated in FIG. 2. (Referring to FIGS. 1 and 2, the origin 201 of the x-axis in FIG. 2 represents the top surface 130 of the semiconductor substrate 102.) Referring to FIG. 2, the buried amorphization implant profile 200 is disadvantageous because an amorphization implant profile that is buried results in a doped junction with higher sheet resistance. In addition, the buried amorphization implant profile 200 has a first **dislocation** interface 202 and a second **dislocation** interface 204 where the concentration of the amorphizing implant species rapidly diminishes. Two such **dislocation** interfaces 202 and 204 may result in a doped junction with higher sheet resistance.

Detailed Description Text - DETX (6):
In addition, the projection ranges of the plurality of amorphizing implant profiles 402, 404, and 406 are controlled such that a top of the first implant

profile 400 is substantially at the top surface 130 of the semiconductor
substrate 102. In that case, only one **dislocation** interface results at a first
depth 410 of the first implant profile 400 where the concentration of the
amorphizing implant species rapidly diminishes. The first depth 410 of the
first implant profile 400 defines an amorphous region within the semiconductor
substrate 102 formed by implantation of the amorphizing implant species.

Detailed Description Text - DETX (8):
In this manner, by forming an implant profile 400 that is substantially
box-shaped for the implantation of the amorphizing implant species, the sheet
resistance of the doped junction is minimized because of the more uniform
concentration of the amorphizing implant species within the amorphous region.
Referring to FIGS. 2 and 4, because the amorphizing implant species is already
relatively uniformly distributed within the amorphous region of the present
invention, the activation temperature and the activation time of the RTA (Rapid
Thermal Anneal) process may be decreased. For example, the RTA process may use
a relatively low temperature in a range of approximately 550.degree. Celsius
to 700.degree. Celsius for a relatively short time period of 60 seconds. Such
lower activation temperature and activation time results in less thermal
diffusion and thus in a shallower doped junction. Furthermore, referring to
FIGS. 2 and 4, because the implant profile 400 of the present invention has
only one **dislocation** interface 410 (instead of two **dislocation** interfaces 202
and 204 in the prior art of FIG. 2), the sheet resistance of the doped junction
of the present invention is further minimized.